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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,580	10/30/2003	Shuichi Takahashi	492322014400	7212

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/696,580	TAKAHASHI ET AL.
	Examiner	Art Unit
	Dao H. Nguyen	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 10/30/2003 through 03/26/2004.

Claims 1-8 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 10/30/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Foreign Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The specification is objected to for the following reason: In the specification, page 5, line 22, the characters "Tthe" should be changed to –The--. Appropriate correction is required.

The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim(s) 1, and 5-6 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,537,877 to Ishida.

Regarding claim 1, Ishida discloses a nonvolatile semiconductor memory device, as shown in figs. 1, 8c, comprising:

a plurality of memory transistors;

a plurality of insulating layers 20, 32, 38 (fig. 8c) disposed over the transistors;

a plurality of metal layers 31a, 36a, BL1, each of the metal layers 31a, 36a, BL1 being disposed on one of the insulating layers 20, 32, 38; and

a plurality of metal plugs 22a, 34a, 39a disposed over corresponding memory transistors, each of the metal plugs 22a, 34a, 39a filling in a contact hole formed in one of the insulating layers and electrically connecting the metal layers disposed on a top side and a bottom side of the corresponding insulating layer,

wherein a top metal layer BL1 of the plurality of metal layers is configured to provide bit lines that correspond to the memory transistors, the metal plugs 22a, 34a, 39a are vertically aligned, and one of the insulating layers (layer 38) is configured so that one of the memory transistors is connected to a corresponding bit line BL1 when a metal plug 39a corresponding to said one of the memory transistors is provided in said one of the insulating layers.

Regarding claim 5, Ishida discloses a nonvolatile semiconductor memory device, as shown in figs. 1, 8c, comprising:

a plurality memory transistors;

a first insulating layer 20 disposed on the memory transistors;

a plurality of first metal plugs 22a filling in contact holes formed in the first insulating layer 20, each of the memory transistors being connected to one of the first metal plugs 22a;

a first metal layer 31a disposed on the first metal plugs 22a;

a second insulating layer 32 disposed on the first metal layer 31a;

a plurality of second metal plugs 34a filling in contact holes formed in the second insulating layer 32, each of the first metal plugs 22a being connected to one of the second metal plugs 34a through the first metal layer 31a;

a second metal layer 36a disposed on the second metal plugs 34a;

a third insulating layer 38 disposed on the second metal layer 36a; and

a third metal layer BL1 disposed on the third insulating layer 38 and providing bit lines, wherein a plurality of third metal plugs 39a filling in contact holes formed in the third insulating layer 38 are arranged so that one of the memory transistors is connected to a corresponding bit line BL1 when a third metal plug 39a corresponding to said one of the memory transistors is provided in the third insulating layer 38, and the first metal plugs 22a, the second metal plugs 34a, the third metal plugs 39a, and the memory transistors are vertically aligned for the memory transistors that have corresponding third metal plugs 39a.

Regarding claim 6, Ishida discloses a nonvolatile semiconductor memory device, as shown in figs. 1, 8c, comprising:

a plurality memory transistors;

a first insulating layer 20 disposed on the memory transistors;

a plurality of first metal plugs 22a filling in contact holes formed in the first insulating layer 20, each of the memory transistors being connected to one of the first metal plugs 22a;

a first metal layer 31a disposed on the first metal plugs 22a;

a second insulating layer 32 disposed on the first metal layer 31a;

a second metal layer 36a disposed on the second insulating layer 32;

a third insulating layer 38 disposed on the second metal layer 36a;

a plurality of third metal plugs 39a filling in contact holes formed in the third insulating layer 38, each of the third metal plugs 39a being disposed on one of the memory transistors; and

a third metal layer BL1 disposed on the third metal plugs 39a and providing bit lines,

wherein a plurality of second metal plugs 34a filling in contact holes formed in the second insulating layer 32 are arranged so that one of the memory transistors is connected to a corresponding bit line BL1 when a second metal plug 34a corresponding to said one of the memory transistors is provided in the second insulating layer 32, and the first metal plugs 22a, the second metal plugs 34a, the third metal plugs 39a and the memory transistors are vertically aligned for the memory transistors that have corresponding second metal plugs.

7. Claim(s) 1-4 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,990,507 to Mochizuki et al.

Regarding claim 1, Mochizuki discloses a nonvolatile semiconductor memory device, as shown in figs. 2,19-23, comprising:

a plurality of memory transistors;

a plurality of insulating layers 10, 30 disposed over the transistors;

a plurality of metal layers 36, 38, each of the metal layers 36, 38 being disposed on one of the insulating layers 10, 30 respectively; and a plurality of metal plugs (plug 33, and vertical portion of wiring 38 above metal layer 36) disposed over corresponding memory transistors, each of the metal plugs filling in a contact hole formed in one of the insulating layers 10, 30 and electrically connecting the metal layers 38, 26 respectively disposed on a top side and a bottom side of the corresponding insulating layer 30,

wherein a top metal layer 38 or BL of the plurality of metal layers is configured to provide bit lines BL that correspond to the memory transistors, the metal plugs are vertically aligned, and one of the insulating layers (layer 30) is configured so that one of the memory transistors is connected to a corresponding bit line BL when a metal plug (vertical portion of wiring 38) corresponding to said one of the memory transistors is provided in said one of the insulating layers (layer 30). See also col. 26, line 13 to col. 30, line 67.

Regarding claim 2, Mochizuki discloses the nonvolatile semiconductor memory device wherein the insulating layer 30 configured for memory transistor connection is a top insulating layer of the plurality of the insulating layers. See figs. 2, and 19-23.

Regarding claims 3 and 4, Mochizuki discloses the nonvolatile semiconductor memory device wherein a size of the metal plugs filling in the contact holes in a top insulating layer 30 of the plurality of insulating layers is larger than a size of the metal

plugs filling in the contact holes in an insulating layer of the plurality of insulating layers 10 that is not the top insulating layer (metal plugs 33 are smaller than the plugs (vertical portion of 38) above it by two times the thickness of the TiN barrier 111 (see fig. 20, and col. 29, lines 36-42; col. 30, lines 39-52).

Claim Rejections - 35 U.S.C. § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim(s) 5-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,990,507 to Mochizuki et al., in view of the following remarks.

Regarding claim 5, Mochizuki discloses a nonvolatile semiconductor memory device, as shown in figs. 2, 17-23, comprising:

a plurality memory transistors;

a first insulating layer 10 disposed on the memory transistors;

a plurality of first metal plugs 33 filling in contact holes formed in the first insulating layer 10, each of the memory transistors being connected to one of the first metal plugs 33;

a second insulating layer 13 (figs. 20/22) disposed on the first metal plugs 33;

a plurality of second metal plugs 133 filling in contact holes formed in the second insulating layer 13, each of the first metal plugs 33 being connected to one of the second metal plugs 133;

a second metal layer 36 disposed on the second metal plugs 133;

a third insulating layer 30 disposed on the second metal layer 36; and

a third metal layer 38 or BL disposed on the third insulating layer 30 and providing bit lines BL,

wherein a plurality of third metal plugs (vertical plug formed in the third insulating layer 30, between the second metal layer 36 and the third metal layer 38) filling in contact holes formed in the third insulating layer 30 are arranged so that one of the memory transistors is connected to a corresponding bit line BL when a third metal plug corresponding to said one of the memory transistors is provided in the third insulating layer 30, and the first metal plugs 33, the second metal plugs 133, the third metal plugs and the memory transistors are vertically aligned for the memory transistors that have corresponding third metal plugs. See also col. 26, line 13 to col. 30, line 67.

In the embodiment illustrated by fig. 20, Mochizuki does not disclose a first metal layer being disposed on the first metal plugs 33 and connecting the first metal plugs33 to the third metal plugs 133.

However, in other embodiments, for example, in embodiment(s) illustrated by figs. 17, 19, Mochizuki does disclose a first metal layer 36 being disposed above the first metal plugs 33 and connecting the first metal plugs 33 to metal plugs above it.

Therefore, It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the invention of Mochizuki illustrated in figs. 20, 22, to further include a first metal layer, as that illustrated in figs. 17, 19 of Mochizuki, being disposed above the first metal plugs 33 and connecting the first metal plugs 33 to metal plugs 133, because those skilled in the art will recognize that such modification and variations could be made easily and would involve only routines skills in the art, and it can be made without departing from the spirit of the invention of Mochizuki.

Regarding claim 6, Mochizuki discloses a nonvolatile semiconductor memory device, as shown in figs. 2, 17-23, comprising:

a plurality memory transistors;

a first insulating layer 10 (fig. 20) disposed on the memory transistors;

a plurality of first metal plugs 33 filling in contact holes formed in the first insulating layer 10, each of the memory transistors being connected to one of the first metal plugs 33;

a second insulating layer 13 disposed on the first metal plugs 33 ;

a second metal layer 36 disposed on the second insulating layer 13;

a third insulating layer 30 disposed on the second metal layer 36;

a plurality of third metal plugs (vertical plug formed in the third insulating layer 30, between the second metal layer 36 and the third metal layer 38) filling in contact holes

formed in the third insulating layer 30, each of the third metal plugs being disposed on one of the memory transistors; and

a third metal layer 38 or BL disposed on the third metal plugs and providing bit lines BL, wherein a plurality of second metal plugs 133 filling in contact holes formed in the second insulating layer 13 are arranged so that one of the memory transistors is connected to a corresponding bit line BL when a second metal plug 133 corresponding to said one of the memory transistors is provided in the second insulating layer 13, and the first metal plugs 33, the second metal plugs 133, the third metal plugs and the memory transistors are vertically aligned for the memory transistors that have corresponding second metal plugs. See also col. 26, line 13 to col. 30, line 67.

In the embodiment illustrated by fig. 20, Mochizuki does not disclose a first metal layer being disposed on the first metal plugs 3.

However, in other embodiments, for example, in embodiment(s) illustrated by figs. 17, 19, Mochizuki does disclose a first metal layer 36 being disposed above the first metal plugs 33 and connecting the first metal plugs 33 to metal plugs above it.

Therefore, It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the invention of Mochizuki illustrated in figs. 20, 22, to further include a first metal layer disposed above the first metal plugs 33, as that illustrated in figs. 17, 19 of Mochizuki, to connect the first metal plugs 33 to metal plugs 133, because those skilled in the art will recognize that such modification

and variations could be made easily and would involve only routines skills in the art, and it can be made without departing from the spirit of the invention of Mochizuki.

Regarding claims 7 and 8, Mochizuki discloses the nonvolatile semiconductor memory device wherein a size of the third metal plugs is larger than a size of the second metal plugs and a size of the first metal plugs.

Mochizuki does not discloses that a size of the second metal plugs and a size of the third metal plugs are both larger than a size of the first metal plugs.

However, it would have been obvious to one of ordinary skill in the art to modify the size of the second metal plugs to be as that of the third metal plugs so that sizes of both of the third metal plugs and the second metal plugs are larger than that of the first metal plugs, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Conclusion

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
September 27, 2005